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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,728	06/26/2003	Brendan K. Bridgford	X-1216 US	5830

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EXAMINER	
RIAD, AMINE	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,728	BRIDGFORD, BRENDAN K.	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claims 1-17 have been presented for examination.

Claims 1-17 have been rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 3, 7, 8, 9, 10, 11, 14, 15, 16, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lindholm U.S. Patent 6,553,523.

In regard to claims 1, and 16 Lindholm discloses a method for debugging a configuration process of a programmable logic device (Figure 1; Item 100) and (Column 2;lin 52-53) comprising: initiating the configuration process for the programmable logic device (Column 3; line 6-9); capturing configuration process signals in the programmable logic device (Column 3; line 13-17 [read back plays the role of capturing]); transferring the captured configuration process signals to a configuration analyzer (Column 3; line 18-19 the host is considered the analyzer) and (Figure 1; item 104); and analyzing the transferred configuration

process signals using the configuration analyzer (Column 5; line 57-59 [comparing means analyzing]).

In regard to claim 2, Lindholm disclose the method of claim 1 further comprising programming a configuration device (Figure 1; item 104 and Column 2; line55-56) coupled to the programmable logic device with a configuration bitstream (Figure 1; item 132).

In regard to claim 3, Lindholm discloses the method of claim 2 wherein initiating the configuration process comprises causing the programmable logic device to send normal configuration process signals to the configuration device, thereby causing the configuration device to provide the configuration bitstream (Column 3; 6-7 when the microcontroller functionally interacts with the PLD that means the two devices work some kind of handshake to enable communication. The handshake process tells the sending device that the receiving device is ready by sending signal from the receiving device in this case the PLD.)

In regard to claim 7, Lindholm disclose the method of claim 1 wherein analyzing the transferred configuration process signals comprises comparing the transferred configuration process signals with expected configuration process signals (Column 5; line 57-58).

In regard to claim 8, Lindholm discloses the method of claim 7 wherein if the transferred and the expected configuration do not match then correcting the configuration process (Column 2; line 27-29) [Since the host evaluates the proper configuration it is inherent that the host corrects the error because it is the host that configures the PLD].

In regard to claim 9, Lindholm discloses a system comprising:
a programmable logic device (Figure 1; item 102);
a configuration device (host 104) coupled to the programmable
logic device for providing a configuration bitstream to the programmable logic device (Figure 1; item 130); and a configuration analyzer coupled to the programmable logic device for controlling the I/O pins of the programmable logic device (Figure 1; item 128), and analyzing configuration process signals received at the programmable logic device (Figure 1; item 104).

In regard to claim 10, Lindholm discloses the system of claim 9 wherein the configuration device is a nonvolatile memory (Figure 1; item 104 since the host is a computer which holds software it has some kind of nonvolatile memory such as a hard drive where the software can be stored).

In regard to claim 11, Lindholm discloses the system of claim 9 wherein the programmable logic device is a field programmable gate array (Column 7; line 58).

In regard to claim 14, Lindholm discloses the system of claim 9 wherein the analyzer comprises a computer running a program for analyzing the configuration data (Column 2; line 25-27 [the host compares means analyzes]).

In regard to claim 17, Lindholm discloses a configuration analyzer for debugging a configuration process of a programmable logic device comprising: means for stepping through the configuration process (Column 2;line 24 [Software 101 receives a user design as well as read back data and that means stepping through configuration]); means for capturing configuration process signals received by the programmable logic device at each step (Column 3; line 13-17 [read back plays the role of capturing]) ; and means for comparing the captured configuration process signals with expected configuration process signals(Column 5; line 57-59).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lindholm US patent 6,553,523 in view of Turner US patent 6,629,311.

In regard to claim 4, Lindholm discloses the method of clam 1.

Lindholm does not disclose initiating the configuration process by accessing the programmable logic device through a JTAG interface.

Turner teaches initiating the configuration process that comprises accessing the programmable logic device through a JTAG (Column 2; line 33-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate initiating the configuration by accessing the PLD through a JTAG interface of Turner into the method of debugging of Lindholm. A person of ordinary skill in the art would have been motivated to make this modification because JTAG INTERFACE utilizes only a small number of pins (only 4), and is very simple to use.

Claims 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindholm US patent 6,553,523 in view of Turner, as applied to claim 4 above, and further in view of JTAG Boundary Scan Basics White Paper.

In regard to claim 5, Lindholm/Turner disclose the method of parent claim 4. Lindholm and turner do not disclose a SAMPLE/PRELOAD and EXTEST instruction on the PLD.

JTAG Boundary Scan Basics White Paper teaches that JTAG requires that all compliant devices must perform the SAMPLE/PRELOAD and EXTEST instructions (Page 2 & 3; Section **Required Instructions**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate initiating the configuration by accessing the PLD through a JTAG interface by executing SAMPLE/PRELOAD and EXTEST instructions of JTAG Boundary Scan Basics White Paper into the method of debugging of Lindholm. A person of ordinary skill in the art would have been motivated to make this modification because it is required for JTAG to function.

In regard to claim 6, Lindholm/Turner disclose the method of parent claim 4.

Lindholm and Turner do not disclose accessing the PLD through a JTAG interface comprises executing a BYPASS instruction on a configuration device coupled to the PLD.

JTAG Boundary Scan Basics White Paper teaches that JTAG requires that all compliant devices must perform the BYPASS instruction (Page 2 & 3; Section **Required Instructions**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate initiating the configuration by accessing the PLD through a JTAG interface by executing BYPASS instructions on a configuration device coupled to the PLD of JTAG Boundary Scan Basics White Paper into the method of debugging of Lindholm. A person of ordinary skill in the art would have been motivated to make this modification because it is required for JTAG to function.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lindholm US patent 6,553,523 in view of Khu US patent 5,805,607.

In regard to claim 12, Lindholm discloses the system of claim 9.

Lindholm does not disclose a programmable logic device that comprises a boundary scan register.

Khu teaches a programmable logic device which comprises a boundary scan (Figure 1; items 14a-14f)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the boundary scan register of Khu into the PLD of Lindholm. A person of ordinary skill in the art would have been motivated to make this modification because one key advantage of the boundary scan is that it allows arbitrary data to be serially scanned into a device's boundary scan register with each bit position corresponding to an input or output terminal of the device.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lindholm US patent 6,553,523 in view of Veenstra US patent 6,704,889.

In regard to claim 13, Lindholm discloses the system of claim 9.

Lindholm does not disclose the programmable logic device and the analyzer form at least part of a JTAG chain.

Veenstra teaches the programmable logic device and the analyzer form at least part of a JTAG chain (Figure 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the PLD and the analyzer which form at least part of JTAG chain of Veenstra into the system of Lindholm. A person of ordinary skill in the art would have been motivated to make this modification because one key advantage of the JTAG INTERFACE is the fact that it has access to small number of pins (only 4), and very simple to use.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lindholm US patent 6,553,523 in view of Giel patent application publication 2004/0015908.

In regard to claim 15, Lindholm discloses the system of parent claims 14, and 9 Lindholm does not disclose an analyzer that comprises a database of known configuration problem.

Giel teaches that the analyzer comprises a database of known configuration problems (Page 2; Paragraph 24 information means configuration problems) and (Figure 2; item 804).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the analyzer, which comprises a database of known configuration problems into the system of Lindholm. A person of ordinary skill in the art would have been motivated to make this modification because it speeds up the process of debugging a PLD.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S patent 6,748,456 teaches most of the limitations, but lacks the capturing of configuration data from the PLD, on the other hand U.S. patent 6,389,558 contains some elements, but lacks an important element, which is debugging the configuration See PTO 892.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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